***DSD LAB SESSION 3***

*Design and simulate 2 to 4-line Decoder and modify the same to construct 3 to 8-line Decoder using dataflow modeling in Verilog HDL*

***2x4 Line Decoder***

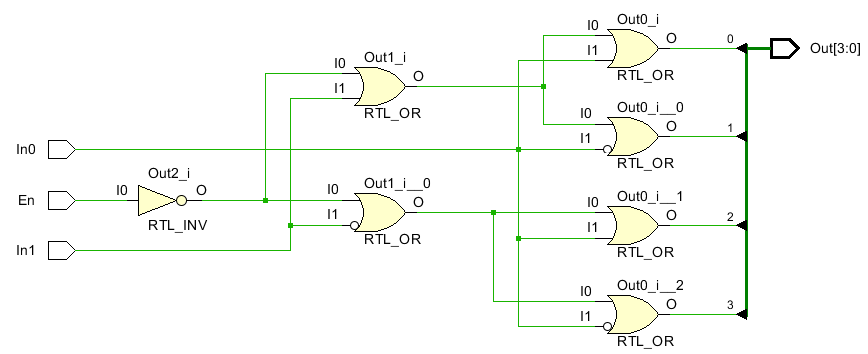
POS (Product of Sum) Equations:

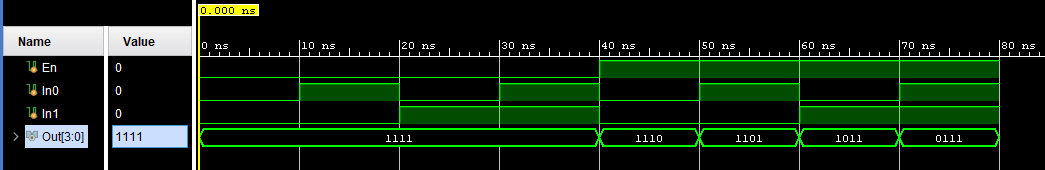
Out[0] = ~En | In1 | In0;

Out[1] = ~En | In1 | ~In0;

Out[2] = ~En | ~In1 | In0;

Out[3] = ~En | ~In1 | ~In0;

******

******

***3x8 Line Decoder***

